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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ROY, SIKHA	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,723	RODRIGUEZ ET AL.	
	Examiner	Art Unit	
	Sikha Roy	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☐ Claim(s) *1-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The Amendment, filed on February 4, 2005 has been entered and is acknowledged by the Examiner.

The Amendment, overcomes the rejection of claims 22, under 35 U.S.C. § 112, second paragraph.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-22 and 24, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 99/17330 to Cooper and further in view of U.S. Patent 5,766,053 to Cathey et al.

Regarding claim 1 Cooper discloses (Figs. 1 and 15, page 2 lines 1-8, page 3 lines 5-20, claim 1) a visual display 100 comprising a cathode plate including a substrate 1_1, 1_2 and emission layer 3 on one face of the substrate, the emission layer

having a multiplicity of emitters and gates arranged as an array of emission pixels, conductive connections in the emission layer to the and gates, the substrate having conductive vias 17 provided through the substrate to at least some of the conductive connections in the emission layer 3 for electrical connection to emitters and gates, an anode plate (glass front face plate) 51, a back plate (back substrate layer) 1_4, the cathode plate being carried on the front side of the back plate, the back plate being continuous across the backside of the cathode plate and a frame (carrier) 40 connecting the back plate 1_4 to the anode plate (page 5 lines 14,15).

Claim 1 differs from Cooper in that Cooper does not disclose a separate back plate.

Cathey in analogous art of flat-panel field emission display panel discloses (Fig. 1 column 4 lines 31-41) flowable connection (rear positioning spacer made of frit seal) 27 is made around the back edge of the cathode plate 16 to a separate back plate 14 isolating a thin gap 36 between the two components. The back plate 14 is continuous across the backside of the cathode plate 16. Cathey further discloses that this configuration creates a rearward vacuum space behind the cathode plate and a forward vacuum space in front of the cathode plate and hence the cathode plate is not subjected to the differential pressure on opposite sides. This embodiment eliminates pressure differential between the sides of the cathode plate. This reduces structural requirements, eliminating the need for distributed spacers.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a separate back plate and the back side of the cathode plate being

carried on the front side of the back plate isolating a thin gap between the cathode plate and the back plate of Cooper as taught by Cathey for eliminating pressure differential between the sides of the cathode plate and hence reducing structural requirements, eliminating the need for distributed spacers.

Referring to claim 2 Cooper discloses (Fig. 14, page 18 lines 5-10) the frame (carrier wall) 40 extends peripherally around the cathode plate.

Regarding claim 3 Cooper discloses (page 5 lines 24, 25) the frame is soldered to the back plate.

Regarding claim 4 the recitation of 'frame joined to the back plate by frit sealing' is drawn to a process of manufacturing which is incidental to the claimed apparatus. It is well established that a claimed apparatus cannot be distinguished over the prior art by a process limitation. Consequently, absent a showing of an unobvious difference between the claimed product and the prior art, the subject product-by-process claim limitation is not afforded patentable weight (see MPEP 2113). Therefore, it is the position of the examiner that it would have been obvious to one of ordinary skill in the art that the visual display disclosed by Cooper is at least a fully functional equivalent to the Applicant's claimed invention.

Regarding claim 5 Cooper discloses (page 5 lines 14-22) the frame (carrier) separate from the back plate with L-shape, one limb extending towards the anode plate.

Claim 5 differs from Cooper in that Cooper does not exemplify the frame and the back plate provided as a single structure.

It would have been obvious to one of ordinary skill in the art at the time of invention to make the frame and the back plate as single structure since it has been held that forming in one piece an article which has formerly been formed in separate pieces and put together involves only routine skill in the art. Furthermore this configuration with the frame and the back plate as single structure would eliminate the step of aligning and joining the frame and the back plate thus providing simpler manufacturing of the display.

Regarding claim 6 Cooper discloses (page 4 line 7, page 6 lines13-15) the frame 40 and back plate are laminated from multiple layers of ceramic material.

Regarding claim 7 Cooper discloses (page 9 lines 5-24) the layers are laminated and compressed together in 'green state' and then fired at elevated temperature to sinter the materials.

Regarding claim 8 Cooper discloses (page 19 lines 20-23) that the back plate 1_4 is pressure tight to atmospheric pressure and the atmospheric pressure acts on the back of the back plate and front of the anode plate.

Regarding claim 9 Cooper discloses (claims 38,39) array of spacers including vias and contact tracks for connecting the phosphor pixels to the drivers between the anode plate and the emission device.

Cooper does not disclose the frame incorporating a network of vias and interconnection tracks for electrical connection of the anode.

The frame (carrier) in the display device of Cooper provides the connection between the back plate and the anode plate and acts as a spacer. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to replace the spacers with the frame connecting the back plate and the anode plate having vias and contact tracks for connecting the phosphor pixels with the driving contacts carried on the emission device.

Referring to claim 10 Cooper discloses (claims 6, 12 Fig.6 page 13 lines 1-8) substrate of the cathode plate is a multilayer substrate having a front substrate layer and an additional substrate layer with conductive vias 20 provided through the front layer and each additional layer and with electrical interconnection tracks (connection strips) 19. Cooper further discloses the arrangement of adjacent layers with interconnection tracks and vias is such that the front layer via is off-set from the back one (vias in zig zag array with gaps in between). The vias being not co-axial provides greater assurance of vacuum tightness.

Referring to claim 11 Cooper discloses the arrangement of vias and electrical interconnection tracks in a multi layer substrate, the adjacent layers being such that the vias in two layers are aligned (page 14 lines 1,2).

Regarding claim 12 Cooper discloses (Figs. 9 and 10 page 15 lines 22-24) the substrate of the cathode plate can have a single ceramic layer with an emission layer 503 built up on it.

Regarding claim 13 Cooper discloses the claimed invention except for the cathode plate having a thicker foundation layer. It would have been obvious matter of design choice to have thicker foundation layer since applicant has not disclosed that thicker foundation layer solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the multilayers of the substrate in cathode plate having same thickness and then fired as disclosed by Cooper.

Regarding claim 14 Cooper discloses the claimed invention except for the back plate having a thicker foundation layer. It would have been obvious matter of design choice to have thicker foundation layer since applicant has not disclosed that thicker foundation layer solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the multilayers of the substrate in back plate having same thickness and then fired as disclosed by Cooper.

Regarding claim 15 Cooper discloses (page 13 lines 1-6 page 16 lines 10-13, Figs. 11,12) the vias in the back plate layers are arranged to spread or fan out towards the next layer for so that the connection strips can be connected to driver chip contacts. As with substrate layers in cathode plate, vias in back plate can be arranged such that vias in the front layers being off-set with those in the next adjacent layer.

Regarding claim 16 it is clearly evident from Fig. 1 that the back plate (comprising 1_3, 1_4) has vias in a front layer positioned to connect with vias in the back of the cathode plate (1_1, 1_2).

Regarding claim 17 Cooper discloses (claim 9) in Fig. 1 that the display includes connection tracks 19 on either of the back plate front layer or the cathode plate back layer.

Referring to claims 18 and 19 Cooper discloses (page 8 lines 10-15) the vias on the back plate front layer or cathode plate back layer are filled with conductive material and the tracks are positioned to interconnect respective vias. Cooper does not disclose the inter connection made by solder or ball grid array.

The selection of known material for a known purpose is generally within the skill of the art. It would have been obvious to use solder or ball grid array for electrically connecting vias and the tracks on cathode plate and back plate because the selection of solder (or ball grid array) for purpose of adhesion and electrical connection is within the skill of the art. Furthermore Cooper discloses using high temperature solders for connecting contact pad and tracks 21,22 to the substrate 1(Fig. 15).

Regarding claim 20 Cathey discloses (Fig. 1 column 4 lines 31-41) flowable connection (rear positioning spacer made of frit seal) 27 is made around the back edge of the cathode plate 16 to the back plate 14 isolating a thin gap 36 between the two components.

Regarding claim 21 Cathey discloses the flowable connection is of glass frit.

Claim 22 recites the same limitation as of claim 18 and hence is rejected for the same reason. Furthermore Cooper discloses (page 24 lines 3-5) high temperature solder (having melting point of 300°C) used for providing electrical connections.

Regarding claim 24 Cooper discloses that the anode plate (front plate) is sealed to the frame (carrier) by a sealing wall of glass frit.

Regarding claim 25 Cooper discloses anode plate sealed to the frame by fused frit seal. Cooper does not disclose fused solder for sealing the anode plate to the frame. It is well within the teaching of art to use fused solder for electrical connection between two components. The selection of known material for a known purpose is generally within the skill of the art. Therefore it would have been obvious to use fused solder for sealing the anode plate to the frame for joining the two and providing electrical connection.

Allowable Subject Matter

Claim 23 is allowed over the prior art of record.

The reason for allowing claim 23 has already been cited by the examiner in the previous office action.

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sikha Roy whose telephone number is (571) 272-2463. The examiner can normally be reached on Monday-Friday 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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